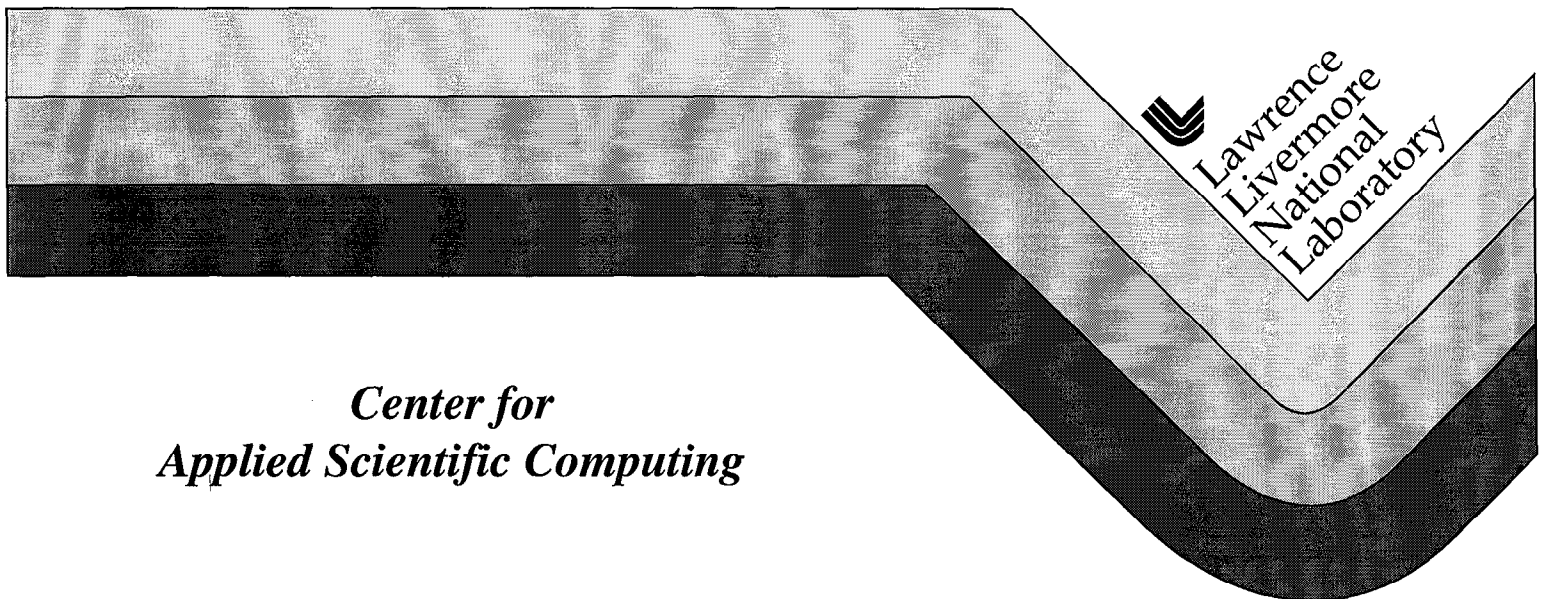


Motion Description for Data Compression and Classification

Martin Lades
Lawrence Livermore National Laboratory



*Center for
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M. Lades

Data compression and processing of image sequences are becoming increasingly important in the era of the information superhighway. This project aims at the development and proof-of-principle of new methods for motion extraction, image sequence compression, and motion analysis. These methods will increase the efficiency of recognition systems and various database applications. The early research into such novel concepts at the forefront of computer vision will benefit LLNL and DOE in all areas associated with archived images and image sequence data. Automated security and surveillance applications are also of special interest in this context.

In FY 1997, we started developing a parallel implementation of the face recognition paradigm on the message passing interface (MPI). A parallel implementation is essential to understanding the structure of large image-databases. Our algorithms are now available to interested parties for applications such as scientific data management (SDM). We also are implementing our new algorithms as a growing library of C++ objects.

During FY 1997, we focused our research efforts on designing and delivering hardware. In particular, we (1) established the capability to design new retinas and other very-large-scale integrated (VLSI) hardware at LLNL's Institute for Scientific Computing Research (ISCR) and (2) fabricated prototypes through MOSIS, a University of Southern California center for experimental VLSI design. Leveraging our connections to the analog VLSI research community—particularly connections with the California Institute of Technology, the University of Zurich, and the University of California, San Diego—we collaborated with Southern Illinois University (SIU) to develop a novel silicon retina with mixed signal processing capabilities. The ITTRACS device delivers the equivalent of 50×10^9 operations (50 GOPS) per second. It performs light detection with logarithmic sensitivity, edge extraction, frame differencing, and centroid calculation at very low power (~ 100 mW). Our chip exploits properties of the silicon substrate, such as the subthreshold behavior of transistors for computational purposes. At the same time, it avoids high power consumption by clocking capacitance at high frequencies. Our new chip offers advanced features such as the capability to blank out the signal calculation—e.g., while the platform carrying the sensor updates its

position—and to track several regions independently. We are preparing a record of invention for this chip.

This last fiscal year, we also demonstrated a pilot system that tracks a moving object appearing in its field of view. This two-chip system uses a predecessor of our new retina design to detect the position of the moving object.

Due to our expertise in silicon retina applications, we obtained prototypes of a new silicon retina and a link decoder from our Caltech collaborators. These implementations feature a new integrated bus system called "Address Events," which makes feasible the asynchronous communication of similar chips in a multiprocessor system of similar devices. These prototypes are available for testing.

Non-refereed Publications, etc.

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